Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (currently amended) An operational amplifier comprising:

a first differential transistor pair receiving a differential input signal at their gates,

a first tail current source transistor connected to sources of the first differential transistor pair, wherein the first differential transistor pair has substrates connected to a supply voltage, and

a load transistor pair connected in series with drains of the first differential transistor pair, wherein the load transistor pair has substrates connected to respective sources of the load transistor pair;

a second differential transistor pair having gates connected to respective drains of the first differential transistor pair~~, wherein the second differential transistor pair has substrates connected to respective sources of the second differential transistor pair~~,

a second tail current transistor connected to sources of the second differential transistor pair; and

an output stage connected to the second differential transistor pair.

2. (original) The operational amplifier of claim 1, wherein transistors of the first differential pair are of the same polarity.

3. (original) The operational amplifier of claim 1, wherein transistors of the load transistor pair are of the same polarity.

4. (original) The operational amplifier of claim 1, wherein transistors of the first differential pair and transistors of the load transistor pair are all of the same polarity.

5. (original) The operational amplifier of claim 1, wherein small signal model transconductance of transistors of the first differential pair and small signal model

transconductance of transistors of the load transistor pair are substantially fixed relative to each other.

6. (original) The operational amplifier of claim 1, wherein transistors of the first differential pair are PMOS transistors.

7. (original) The operational amplifier of claim 1, wherein transistors of the load transistor pair are PMOS transistors.

8. (original) The operational amplifier of claim 1, further including a current source connected to a gate of the first tail current source transistor that permits a squeezing of the first tail current source transistor.

9. (original) The operational amplifier of claim 8, wherein the current source includes a third differential transistor pair whose gates are driven by the differential input signal.

10. (original) An operational amplifier comprising:

a first stage inputting a differential input signal;

an input stage including a first differential transistor pair connected the first stage, and a first tail current source transistor connected to sources of the first differential transistor pair; and

an output stage,

wherein the first stage includes:

a second differential transistor pair;

a second tail current source transistor connected to sources of the second differential transistor pair; and

a load transistor pair connected in series with drains of the second differential transistor pair, ~~and~~

wherein substrates of the load transistor pair are connected to their respective sources, ~~and~~

wherein the output stage is connected to the second differential transistor pair, and

wherein the first differential transistor pair has substrates connected to a supply voltage.

11. (original) The operational amplifier of claim 10, wherein transistors of the second differential pair are of the same polarity.

12. (previously presented) The operational amplifier of claim 10, wherein transistors of the load transistor pair are of the same polarity.

13. (previously presented) The operational amplifier of claim 10, wherein all transistors of the second differential pair and transistors of the load transistor pair are of the same polarity.

14. (previously presented) The operational amplifier of claim 10, wherein small signal model transconductance of transistors of the first differential pair and small signal model transconductance of transistors of the load transistor pair are substantially fixed relative to each other.

15. (previously presented) The operational amplifier of claim 10, wherein transistors of the second differential pair are PMOS transistors.

16. (previously presented) The operational amplifier of claim 10, wherein transistors of the load transistor pair are PMOS transistors.

17. (previously presented) The operational amplifier of claim 10, further including an amplifier that extends a normal range of operation of the second tail current source transistor.

18. (previously presented) The operational amplifier of claim 10, wherein the current source includes a third differential transistor pair whose gates are driven by the differential input signal.

19. (previously presented) The operational amplifier of claim 10, wherein the first stage includes:

a second differential transistor pair;

a current source connected to sources of the second differential transistor pair; and

a load transistor pair connected in series with the second differential transistor pair.

20. (previously presented) The operational amplifier of claim 10, wherein the first stage expands a common mode input range of the operational amplifier.